

DERWENT-ACC-NO: 2003-037161

DERWENT-WEEK: 200303

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TITLE: Precharge control circuit

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PRIORITY-DATA: 2000KR-0084097 (December 28, 2000)

PATENT-FAMILY:

PUB-NO	PAGES	PUB-DATE	MAIN-IPC
KR 2002054857 A		July 8, 2002	
001	G11C 007/12		N/A

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO
KR2002054857A	N/A	2000KR-
0084097	December 28, 2000	

INT-CL (IPC): G11C007/12

ABSTRACTED-PUB-NO: KR2002054857A

BASIC-ABSTRACT:

NOVELTY - A precharge control circuit is provided to prevent a malfunction of a main amplifier by controlling a precharge signal.

DETAILED DESCRIPTION - The first delay portion(41) delays a precharge control signal. The first inverter(42) inverts an output of the first delay portion(41). The second inverter(43) inverts an output of

the first inverter(42) and output a precharge delay signal. The first short pulse delay portion(44) outputs a short pulse signal. The first NAND gate performs a logical operation for the precharge delay signal and an output signal of the first short pulse delay portion(44) and outputs a set signal. The third inverter inverts a precharge control signal. The second delay portion(47) delays an output signal of the third inverter(46). The fourth inverter(48) inverts an output signal of the second delay portion(47). The second NAND gate(49) performs the logical operation for an output signal of the third inverter and an output signal of the fourth inverter(48). The fifth inverter(50) inverts an output signal of the second NAND gate(49) and outputs a precharge enable signal. The sixth inverter(51) inverts the precharge enable signal. The second short pulse delay portion(52) outputs the short pulse signal. The third NAND gate(53) outputs a reset signal. A latch portion(54) performs an operation for the set signal, the reset signal, and a reset signal of a memory device. A precharge signal output portion(55) receives an output signal of the latch portion(54) and outputs a precharge signal.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: PRECHARGED CONTROL CIRCUIT

DERWENT-CLASS: U14

EPI-CODES: U14-A07;



